UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,009	02/25/2005	Akiyoshi Fujii	1248-0772PUS1	4652

2292 7590 08/20/2007

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
08/20/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/526,009	FUJII ET AL.	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2007- 30 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9,10,26-30,34 and 35* is/are pending in the application.

4a) Of the above claim(s) *30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9,10,26-29,34 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/30/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Status

1. In the amendments filed on June 1, 2007, claims 7-8, 11-25 and 31-33 were cancelled, claims 1 and 26 were amended, and claim 30 remains withdrawn. Thereby, claims 1-6, 9, 10, 26-29, 34 and 35 are given full consideration in this Office Action.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on June 10, 2007 incorrectly listed the Japanese reference JP-62-143469-A as JP-62-142469. Therefore, Applicant submitted a corrected Form PTO-1449, on June 30, 2007, with the correct Japanese patent number, and requested that this form be substituted for the incorrect one previously filed on June 10, 2007.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 26-29 and 35** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject

matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In lines 2-4 of claim 26, the limitation of "a semiconductor layer that has been etched after a mask material is dropped onto a semiconductor film and a conductor layer are formed on the gate electrode," is not supported by the specification, because in Applicant's specification, the conductor layer is described as a mask used for forming the semiconductor layer. Thus, based on the specification, the conductor layer and mask material are the same element. However, in claim 26, the mask material and the conductor layer are claimed as two different features, and there is no such description in specification supporting these claimed limitations as two different features. Claims 27-29 and 35 depend from claim 26, and thus are also rejected for the same reasons as set forth above.

5. **Claims 1-6, 9, 10, 26-29, 34 and 35** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In lines 2-4 of claim 1, the limitation of "a semiconductor layer that has been etched after a mask material is dropped on a semiconductor film," is unclear and ambiguous, because it appears from the specification, that the semiconductor layer and the semiconductor film are the same element. However, as recited in claim 1, the semiconductor layer and the semiconductor film are claimed as different elements. For examination purposes, "a semiconductor film" will be interpreted as "the semiconductor

layer." Furthermore, the limitation should be rewritten as: "a semiconductor layer, that has been etched after a mask material is dropped onto the semiconductor layer, is formed on the gate electrode via a gate insulation layer;" the addition of commas to the claim sentence would clarify the claimed structure. Claims 2-6, 9, 10 and 34 depend from claim 1, and thus are also rejected.

In lines 2-4 of claim 26, the limitation of "a semiconductor layer that has been etched after a mask material is dropped on a semiconductor film," is unclear and ambiguous, because it appears from the specification, that the semiconductor layer and the semiconductor film are the same element. However, as recited in claim 1, the semiconductor layer and the semiconductor film are claimed as different elements. For examination purposes, "a semiconductor film" will be interpreted as "the semiconductor layer." Furthermore, the limitation should be rewritten as: "a semiconductor layer, that has been etched after a mask material is dropped onto the semiconductor layer, and a conductor layer are formed on the gate electrode via a gate insulation layer;" the addition of commas to the claim sentence would clarify the claimed structure. Claims 26-29 and 35 depend from claim 1, and thus are also rejected.

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claim 1-6, 9, 10 and 34** (as best understood by the Office) are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Furusawa (US 2003/0219934; cited by Applicant).

Regarding claim 1, Furusawa discloses a TFT array substrate **(10, FIG. 10)** comprising:

a thin film transistor section **(T, FIG. 3)** in which a gate electrode **(13, FIG. 10)** is formed on a substrate **(10)**, and

a semiconductor layer **(18a, FIG. 10)** is formed on the gate electrode **(13)** via a gate insulation layer **(16, FIG. 10)**, wherein the semiconductor layer **(18a)** having a shape formed by dropping a droplet **(pg. 7: ¶ [0096]-[0099])**.

Thus, Furusawa teaches all the features of claim 1 as set forth above, including wherein the semiconductor layer **(18a)** has a circular shape formed by dropping a droplet **(FIG. 10)**.

As to the grounds of rejection under section 103(a), the limitation of a "semiconductor layer that has been etched after a mask material is dropped onto the semiconductor layer," is considered a product by process limitation and therefore is given no patentable weight.

Initially, and with respect to claim 1, note that a "product by process" claim is directed to the product per se, no matter how actually made. *In re Thorpe et al.,* 227 USPQ 964, (CAFC, 1985) and the related case law cited therein makes it clear that it is

the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claim or not. As stated in Thorpe:

> Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington,* 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935);

Note that Applicant has burden of proof in such cases as the above case law makes it clear.

Regarding claim 2, Furusawa discloses wherein the gate electrode **(13, FIG. 4)** in the thin film transistor section is a branch electrode **(13)** which is branched out of a main line **(12, FIG. 4; pg. 5: [0064])** of the gate electrode, and the branch electrode **(13)** has an open end protruded from an area for the semiconductor layer **(18a, FIG. 10)**.

Regarding claim 3, the limitation of "a portion protruded from area for the semiconductor layer is smaller in width than a portion confined within the area for the semiconductor layer," is non-critical matter. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the device would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531

F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

Regarding claim 4, Furusawa discloses wherein the thin film transistor section **(T, FIG. 3)** further includes a source electrode **(22)** and a drain electrode **(22)** on the semiconductor layer **(18, 18a)**, and a channel section **(¶ [0099])** is formed between the source and drain electrodes **(22)**, and the portion of the branch electrode **(13)** protruded from the area for the semiconductor layer **(18, 18a)** is formed in contact with one of the source and drain electrodes **(22)**.

Regarding claims 5 and 6, Furusawa discloses wherein the thin film transistor section **(T, FIG. 3)** further includes source and drain electrodes **(22)** on the semiconductor layer **(18, 18a)**, and a channel section **(¶ [0099])** is formed between the source and drain electrodes.

Note that the limitation, wherein "the portion of the branch electrode protruded from the area for the semiconductor layer is formed according to the following formula…variation of dropping amount of the droplet for forming the semiconductor layer and variation of spread of the droplet after dropping…," is drawn to a process by which the product is made. Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Marosi et al.*, 218 USPQ 289; and

particularly *In re Thorpe*, 227 USPQ 964 (CAFC, 1985), all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. **Note that applicant has burden of proof in such cases,** as the above case law makes clear.

Regarding claim 9, Furusawa discloses wherein the thin film transistor section **(T, FIG. 3)** further includes source and drain electrodes **(22)** on the semiconductor layer **(18, 18a)**, and a channel section **(¶ [0099])** is formed between the source and drain electrodes.

Note that the limitation, wherein "the semiconductor layer is formed according to the following formula…variation of dropping amount of the droplet for forming the semiconductor layer and variation of spread of the droplet after dropping…," is drawn to a process by which the product is made. Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964 (CAFC, 1985), all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a

product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. **Note that applicant has burden of proof in such cases** as the above case law makes clear.

Regarding claim 10, Furusawa discloses a liquid crystal display device **(FIG. 11; pg. 7: ¶ [0100]- [0102])** including the TFT array substrate as set forth in claim 1.

Regarding claim 34, Furusawa discloses an electronic device **(FIG. 11; pg. 7: ¶ [0100]- [0102])** including the TFT array substrate as set forth in claim 1.

7. **Claim 26-29 and 35** (as best understood by the Office) are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kawase (US 7,198,885).

Regarding claim 26, Kawase discloses a thin film transistor array substrate **(Figs. 1-8)**, comprising:

a thin film transistor array section **(Figs. 7-8)** in which a gate electrode **(31)** is formed on a substrate **(22, Fig. 1)**, and in which a semiconductor layer **(508, Figs. 7-8)** and a conductor layer **(502, 504)** are formed on the gate electrode **(31)** via a gate insulation layer **(500)**;

wherein the conductor layer **(502, 504; Figs. 7-8)** is formed in contact with the semiconductor layer **(508; FIG. 7)** and one of source and drain electrodes **(28, 32)** of the thin film transistor section, and has a portion formed by dropping a droplet **(col. 12: lns. 42-44)**, wherein the conductor layer and the semiconductor layer **(508, col. 12: lns. 56-59)** having substantially the same shape formed by dropping a droplet **(the**

conductor regions (502, 504) and the semiconductor layer (508) are both formed by the inkjet method (col. 12: lns. 42-59), and thus have substantially the same shape formed by dropping a droplet, as seen in Fig. 7).

Thus, Kawase teaches all the features of claim 1 as set forth above, including wherein the conductor layer **(502, 504)** and the semiconductor layer **(508)** have substantially similar shapes **(FIG. 7)** formed by dropping a droplet **(col. 12: lns. 42-59)**.

As to the grounds of rejection under section 103(a), the limitation of a "semiconductor layer that has been etched after a mask material is dropped onto the semiconductor layer," is considered a product by process limitation and therefore is given no patentable weight.

Initially, and with respect to claim 26, note that a "product by process" claim is directed to the product per se, no matter how actually made. *In re Thorpe et al.,* 227 USPQ 964, (CAFC, 1985) and the related case law cited therein makes it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claim or not. As stated in Thorpe:

> Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington,* 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935);

Note that Applicant has burden of proof in such cases as the above case law makes it clear.

Regarding claims 27 and 28, Kawase discloses wherein the conductor layer is constituted of a metal material mainly containing one of Ag **(col. 12: lns. 16-20)** and the source and drain electrodes are made of Al **(col. 9: lns. 29-32)**.

Regarding claim 29, Furusawa discloses a liquid crystal display device **(FIG. 22)** including the TFT array substrate as set forth in claim 1.

Regarding claim 35, Furusawa discloses an electronic device **(FIG. 22)** including the TFT array substrate as set forth in claim 1.

Response to Arguments

8. Applicant's arguments with respect to claims 1-6, 9, 10, 26-29, 34 and 35 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ak

/Thao X Le/
Primary Examiner, Art Unit 2814